Accelerating Gate Sizing using GPU

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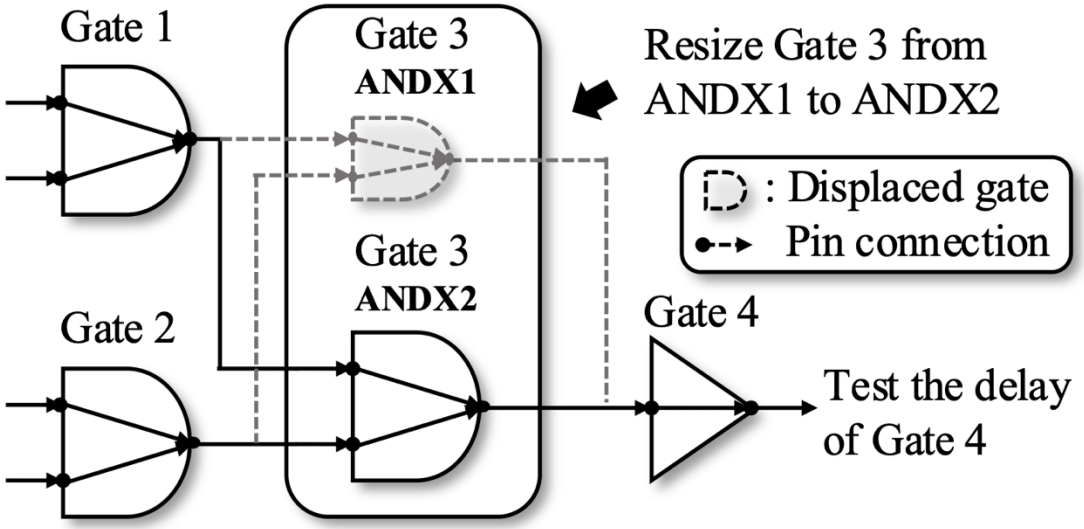
Problem Definition: Gate Sizing

- **Gate sizing** is a critical optimization step in VLSI design that directly impacts circuit performance, power consumption, speed, and area.
- **Goal**: **Select the best cell size** for each gate to achieve optimal trade-offs between timing, power, and area constraints.

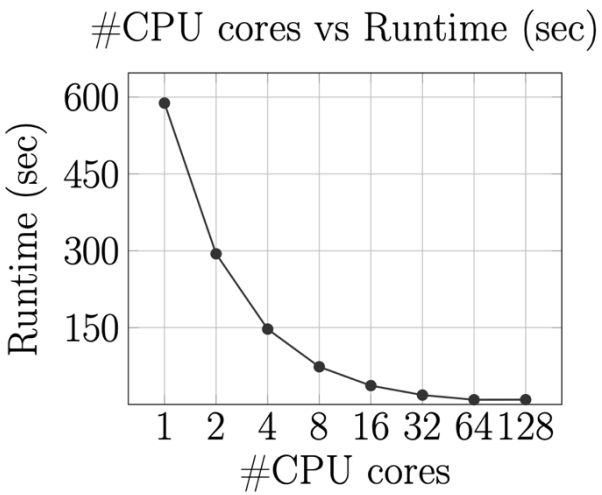


Resize Gate 3 from ANDX1 to ANDX2

- **Benefit**: The gate becomes faster and reduces the timing delay along the critical path.
- **Trade-off**: A larger gate size consumes more area and results in higher power consumption.

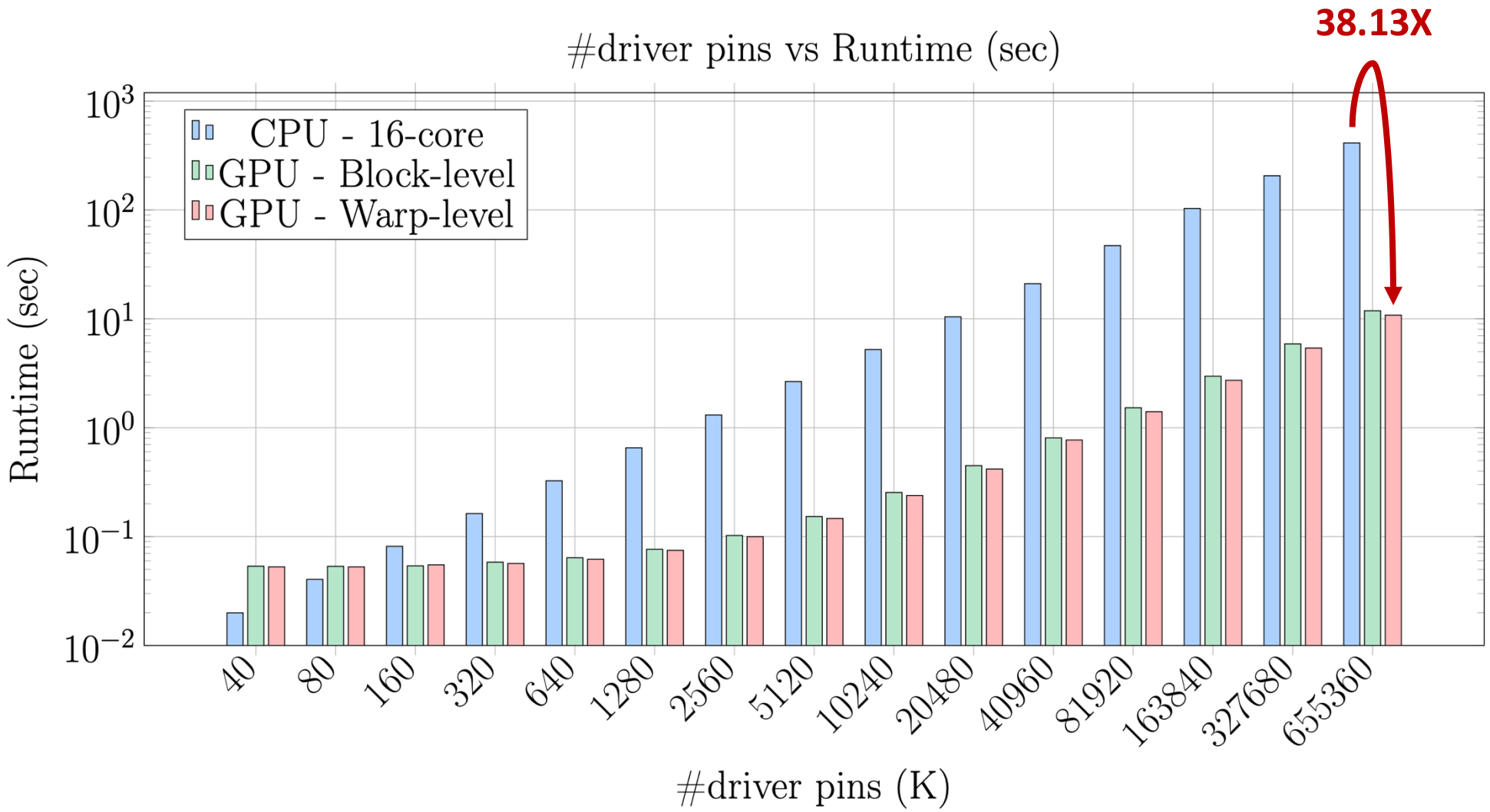
Limitation

- Selecting the best cell size (libcell size) for each gate on the circuit graph is an **optimization problem (NP-hard)**.
- As we know, modern circuit designs are extremely large. In fact, a single circuit can contain millions of gates.
- Today's Industrial tools use **multi-core CPUs** to accelerate gate sizing.
- CPU scalability usually **saturates beyond 16-64 threads**.



- In this work, we accelerate the process of gate sizing on a GPU to overcome CPU scalability limits by proposing **block-level** and **warp-level** algorithms for libcell selection.

Experimental Results



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